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*913*

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/170,625    10/13/98    CHOI

D    8733D-6836

MMC2/0526

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EXAMINER

HAWRANEK, S

ART UNIT

PAPER NUMBER

2823

DATE MAILED:

05/26/00

**Please find below and/or attached an Office communication concerning this application or proceeding.**

**Commissioner of Patents and Trademarks**

# Office Action Summary

Application No.  
09/170,625

Applicant(s)

Choi

Examiner

Scott J. Hawranek

Group Art Unit  
2823



☒ Responsive to communication(s) filed on Mar 20, 2000

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

## Disposition of Claims

☒ Claim(s) 1-36 is/are pending in the application.

Of the above, claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

☐ Claim(s) \_\_\_\_\_ is/are allowed.

☒ Claim(s) 1-36 is/are rejected.

☐ Claim(s) \_\_\_\_\_ is/are objected to.

☐ Claims \_\_\_\_\_ are subject to restriction or election requirement.

## Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on \_\_\_\_\_ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on \_\_\_\_\_ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some\* ☐ None of the CERTIFIED copies of the priority documents have been  
☐ received.

☐ received in Application No. (Series Code/Serial Number) \_\_\_\_\_.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\*Certified copies not received: \_\_\_\_\_

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

## Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 4

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

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## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maekawa (US Pat No. 6,066,547) in combination with Arai et al. (US Pat No. 5,576,222) and Seung-Ik Jun (Aepse '97) and/or Cristoloveanu et al. (SOI).

Maekawa discloses in figures 1-20 and related text forming a TFT forming an amorphous silicon layer as an active layer on a glass substrate or quartz (fig. 8, 14) with an oxide; forming a gate insulating layer (fig. 8, 18) and a gate electrode on the amorphous silicon layer (fig. 8, 20); doping impurities of a first conductive type in the amorphous silicon layer (fig. 8, 22); forming a metal layer of less than 30A (col. 6) on the exposed portions of the amorphous silicon layer (fig. 8, 24); and crystallizing the amorphous silicon layer by applying thermal treatment. With the formation of at least the first electrode prior to the recrystallization step; source/drain regions formed prior to the crystallization step. It is held, absent evidence to the contrary, that the subsequent use of the TFT would require the formation of source/drain contracts in which an

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electric field on the substrate would be generated via the current. See In re Best, 195 USPQ 428 (CCPA 1977) and In re Fitzgerald, 205 USPQ 594 (CCPA 1980).

Examiner takes official notice the selection of PH3 as a dopant is notoriously obvious in the art.

Maekawa teaches forming the gate electrode from a semiconductor film (20) selected from a group consisting of polycrystalline silicon, refractory metals, and other conventional semiconductor materials that are suitable. (col. 5, line 60-65)

Arai et al. (US Pat No. 5,576,222) discloses in figs. 1-7(B) forming an conventional gate electrodes from doped amorphous silicon layer (fig. 2(f), 5') and forming an active layer of amorphous silicon (fig. 2(f), 3') then converting both layers simultaneously into polycrystalline layers which is a conventional semiconductor material. Therefore, it would have been obvious to one of ordinary skill in the art to combine the teachings of Arai et al. with Maekawa for the disclosed intended purpose of forming a gate electrode.

Arai et al. and Maekawa lack anticipation for annealing the amorphous silicon layer into polycrystalline utilizing an electric field to the resultant substrate.

Seung-Ik Jun (Aepse '97) discloses utilizing field aided lateral crystallization (FALC) utilizing a thin layer of nickel as a catalyst (~30Å) at around 500 [C] on and amorphous silicon in order to obtain a high quality film of polycrystalline and other disclosed reasons. It would have been obvious to one of ordinary skill in the art to utilized the FALC in order to obtain a high quality film and combine Jun's teachings with Arai and Maeakawa..

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Cristoloveanu et al. (SOI) discloses in figs. 1-6 and related discloses utilizing FALC in order to achieve polycrystalline silicon from amorphous silicon it would have been obvious to one of ordinary skill in the art to combine the teachings with Critoloveanu with Arai and Maekawa in order to achieve polycrystalline films.

***Response to Amendment***

3. The Declaration filed on 3/16/200 under 37 CFR 1.131 is sufficient to overcome the article entitled "I-V Characteristics of Poly-Silicon TFTs by FALC" published October 13-15, 1997 in Seoul Korea.

***Response to Arguments***

4. Applicant's amendments filed 3/8/00 and 3/20/00 have been fully considered and are persuasive to overcome previous claim objections and 35 U.S.C. 112 rejections.

***Conclusion***

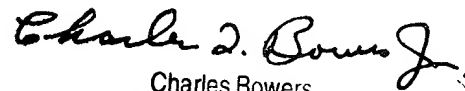
5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott J. Hawranek whose telephone number is (703) 305-0070. The examiner can normally be reached on Monday thru Friday from 8:30 to 6:00 P.M. .

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy, can be reached on (703) 308-4918. The fax phone number for this Group is (703) 308-7722.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-1778.

Scott J. Hawranek  
Art Unit: 2823  
May 25, 2000

  
Charles Bowers  
Supervisory Patent Examiner  
Technology Center 2800